CMS8S3680/69xx Datasheet

Enhanced flash memory 1T 8051 microcontrollers

Rev. 1.0.8

Please note the following CMS IP policy

1. Product features

1.1 Features

- **Compatible with MCS-51 1T command system**
  - The system clock frequency supports up to 48MHz
  - The fastest machine cycle supports 1TSYS @ FSYS≤24MHz
  - The fastest machine cycle supports 2TSYS @ FSYS＝48MHz
- Memory
  - Maximum program FLASH: 16K×8Bit
  - Maximum Data FLASH: 1K×8Bit
  - General RAM: 256×8Bit
  - General XRAM: 1K×8Bit
  - Program FLASH supports partition protection
- **4 oscillation modes**
  - HSI-Internal high-speed oscillation: 48MHz
  - HSE-external high-speed oscillation: 8MHz/16MHz
  - LSE-external low-speed oscillation: 32.768KHz
  - LSI-Internal low-speed oscillation: 125KHz
- **Low voltage reset function（LVR）**
  - 1.8V/2.0V/2.5V/3.5V
- **Low-voltage detection function（LVD）**
  - 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V
- **GPIO**
  - Up to 22 GPIO
  - All digital functions can be assigned to any GPIO
  - Both support up/down resistance function
  - Both support edge (rising edge/falling edge/double edge) interrupt
  - Support wake-up function
- **Interrupt source**
  - Support all external port interrupts
  - Up to 7 timer interrupts
  - Other peripheral interrupts
- **Timer**
  - WDT timer (watchdog timer)
  - Up to 5 timers: Timer0/1, Timer2, Timer3/4
  - LSE Timer (Support sleep wake function)
  - WUT (Wake-up timer)
- **Operating voltage range**
  - 2.1V～5.5V
- **Operating temperature range**
  - -40℃～105℃
- **Buzzer driver**
  - 50% duty cycle, frequency can be set freely
- **Enhanced PWM**
  - 6 channels enhanced PWM
  - 6 mutually independent cycle counters
  - Support independent/complementary/synchronous/group mode
  - Support edge alignment/center alignment
  - Support complementary mode dead zone delay function
  - Support mask function and brake function
- **High-precision 12-bit ADC**
  - All GPIOs (22I/Os) support AD channels
  - Optional reference voltage (1.2V/2.0V/2.4V/3.0V/VDD)
  - Can detect internal 1.2V reference voltage
  - Support hardware trigger start conversion function
  - Support a set of result digital comparison function
- **Two analog comparators (ACMP0/1)**
  - 5 options for positive terminal, internal 1.2V/VDD voltage divider for negative terminal
  - Comparator supports unilateral/bilateral hysteresis
  - Hysteresis voltage optional 10/20/60mV
  - Support comparison output to trigger EPWM brake
  - The internal 1.2V/VDD divider of the negative terminal can be connected to the internal ADC channel
- **Two-way operational amplifier（OP0/1）**
  - Three terminals of each op amp are multiplexed

- BRT (serial port baud rate clock generator)

◆ **Communication module**

- 1xSPI (communication rate up to 6Mb/s)
- 1xI2C (communication rate up to 400Kb/s)
- Up to 2xUART (baud rate up to 1Mb/s)

◆ **Low power mode**

- Idle mode（IDLE）
- Sleep mode（STOP）

with GPIO port

- The positive end supports internal 1.2V input
- Support two modes of op amp/comparator
- Op amp output can be connected to internal ADC channel
- The output of the op amp can be connected to the input of the internal analog comparator
- **Support offset voltage software trimming**

◆ **Programmable gain amplifier（PGA）**

- Support offset voltage software trimming
- With sample and hold circuit (used with ADC)
- Multi-stage gain optional (1/2/4/8/16/32/64/128 times)
- Support single-ended/pseudo-differential input
- PGA output can be connected to the internal ADC channel
- PGA output can be connected to internal analog comparator input

◆ **Support 96-bit unique ID number (UID)**

- Each chip has an independent ID number

◆ **Support two-wire serial programming and debugging**

1.2 Product comparison

Product mode / Peripheral interface		CMS8S3680 -SSOP16	CMS8S6980 -SSOP20	CMS8S6990NA -QFN20 CMS8S6990N -TSSOP20	CMS8S6990 -SSOP24 CMS8S6990 -QFN24
Maximum clock frequency		48 MHz			
Storage module	APROM	8KB	16KB		
	BOOT	0/1/2/4KB	0/1/2/4KB		
	Data FLASH	1 KB			
	RAM	256 B			
	XRAM	512B	1 KB		
Timer	WDT	1			
	Timer0/1	2 (16bit)			
	Timer2	1 (16bit)			
	Timer3/4	2 (16bit)			
	LSE Timer	1 (16bit)			
	WUT	1 (12bit)			
	BRT	1 (16bit)			
Enhanced Digital peripherals	BUZZER	1			
	PWM	6(16bit)			
Communication module	SPI	1			
	I2C	1			
	UART	2	1	2	
Analog module	12bit-ADC (Number of external channels)	14	18	18	22
	ACMP	-	1	2	
	OP	-		2	
	PGA	1	-	1	
GPIOs		14	18	18	22
LVR		1.8V/2.0V/2.5V/3.5V			
LVD		2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V			
Working voltage		2.1~5.5 V			
Operating temperature		-40~105℃			
Encapsulation		SSOP16	SSOP20	QFN20 TSSOP20	QFN24 SSOP24

2. System overview

2.1 System Introduction

The CMS8S3680/69xx series is an 8051 core, a 1T instruction system compatible with MCS-51, and a general IO type 8-bit chip. The operating frequency can reach up to 48MHz. The MCU has the following characteristics:

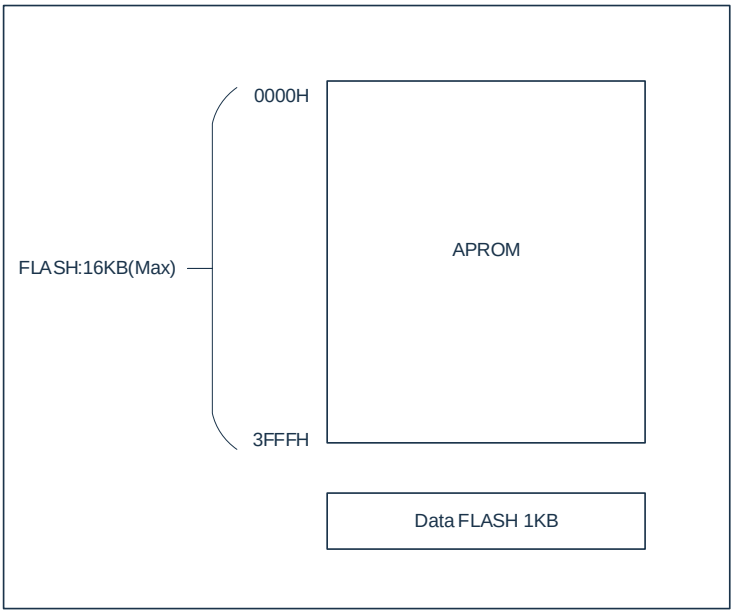
- With a maximum of 16KB program area, 256B RAM space, 1KB XRAM, 1KB data area.
- With four oscillation modes.
- It supports three working modes: normal, idle, and sleep, which can effectively reduce power consumption.
- Built-in low-voltage reset LVR, low-voltage monitoring LVD, watchdog overflow reset and other protection settings can effectively improve the reliability of system operation.
- With multiple interrupt sources such as external interrupts, timed interrupts and other peripheral interrupts, it can respond to external events in a timely manner and improve the utilization of the MCU.
- Digital functions can be assigned to any IO port.
- 9 timers can realize functions such as timing, counting, input capture, output comparison, timing wake-up, and baud rate generator.
- 6-channel 16-bit PWM, supports independent, complementary, and synchronous three-mode output, and has hardware brake function, dead zone control function, mask output and other functions.
- With 1 I2C, 1 SPI, and 2 UART communication modules, it can realize data transmission between the system and other devices.
- It has a high-precision 12-bit ADC and can choose an internal reference voltage, 2 operational amplifiers, 2 comparators, and 1 programmable gain amplifier. Each IO can be used as the input channel of the ADC, and the analog function is more abundant.

2.2 Memory structure

2.2.1 Program memory FLASH

This series has a maximum of 16KB of FLASH storage space, APROM area and BOOT area share the entire FLASH space.

The block diagram of the FLASH space allocation structure is as follows:



CMS8S3680 can configure the size of BOOT, the configuration method is as follows:

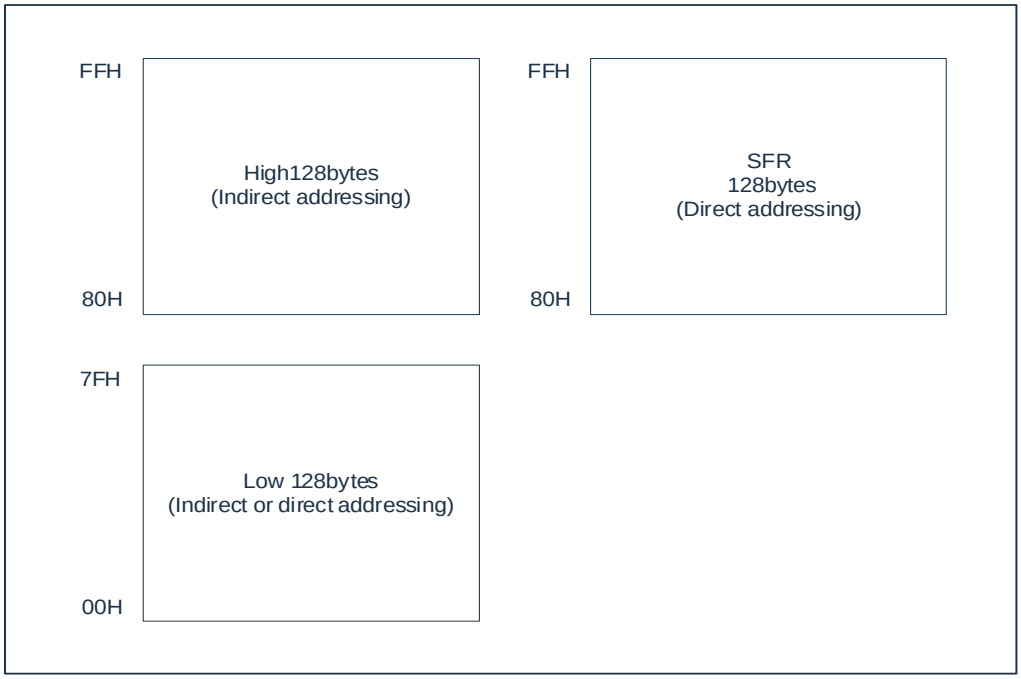
Program storage area				
Address space allocation method	APROM		BOOT	
method0	8K	0000H-1FFFH	--	--
method1	8K	0000H-1FFFH	1K	3C00H-3FFFH
method2	8K	0000H-1FFFH	2K	3800H-3FFFH
method3	8K	0000H-1FFFH	4K	3000H-3FFFH

CMS8S6980/CMS8S6990 can configure the size of BOOT, the configuration method is as follows:

Program storage area				
Address space allocation method	APROM		BOOT	
Method 0	16K	0000H-3FFFH	--	--
Method 1	15K	0000H-3BFFH	1K	3C00H-3FFFH
Method 2	14K	0000H-37FFH	2K	3800H-3FFFH
Method 3	12K	0000H-2FFFH	4K	3000H-3FFFH

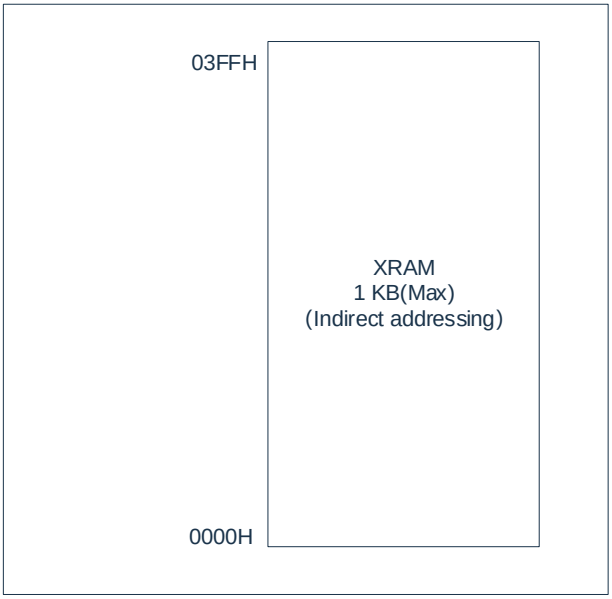
2.2.2 Internal data memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, SFR. The structure diagram of RAM space allocation is shown in the figure below:



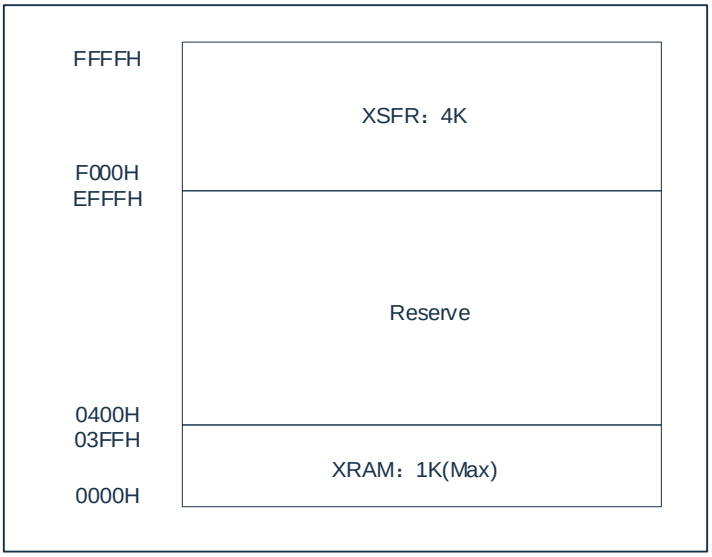
2.2.3 External data memory XRAM

There is a maximum 1KB XRAM area inside the chip, which is not related to RAM/FLASH. The structure diagram of XRAM space allocation is shown in the figure below.



2.2.4 Special function register XSFR

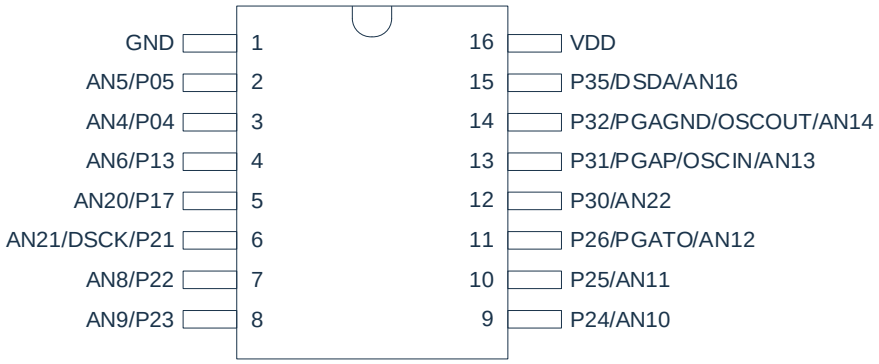
XSFR is a special register shared by the addressing space and XRAM, which mainly includes: port control register and other function control registers. Its addressing range is as follows:



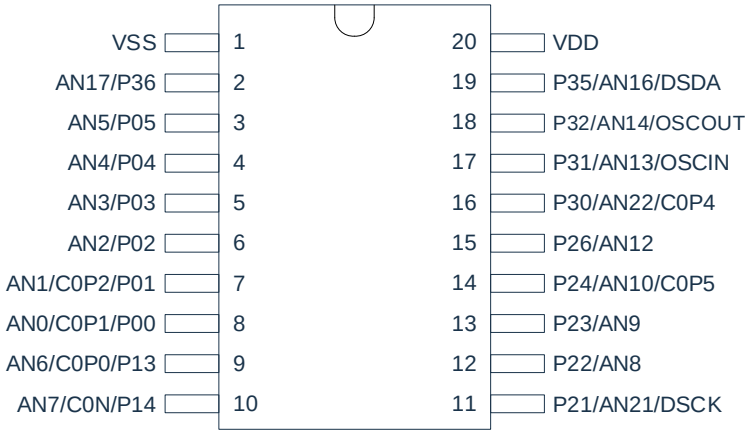
3. Pin definition

3.1 Pin description

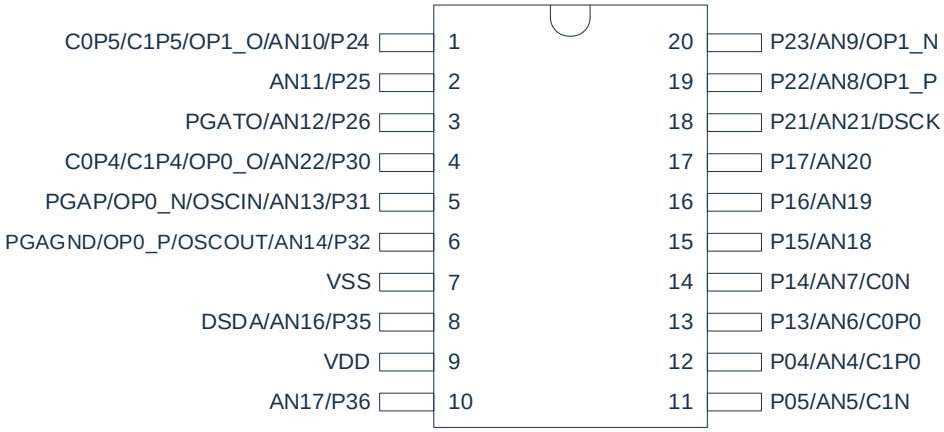
3.1.1 CMS8S3680-SSOP16 Pin diagram



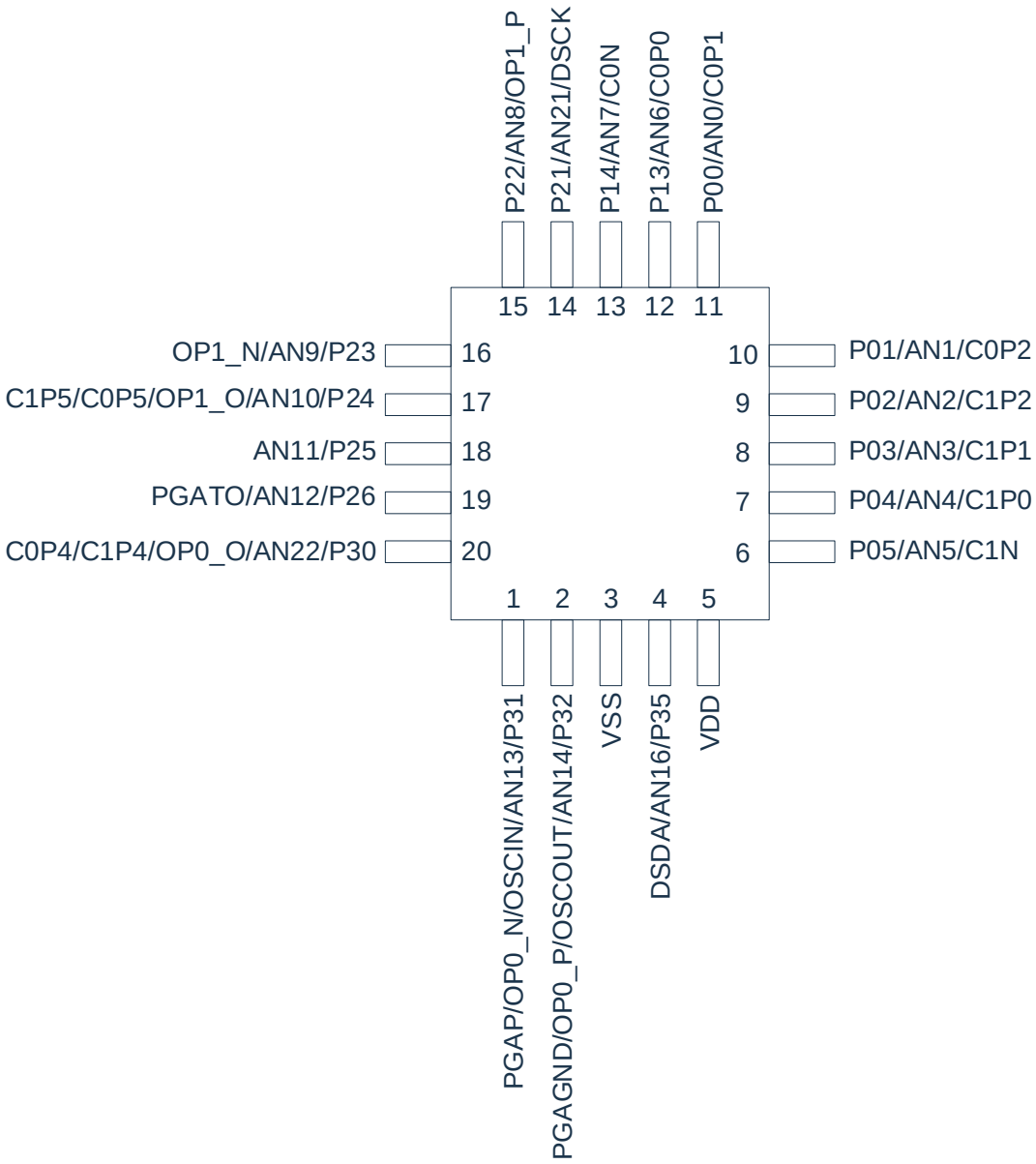
3.1.2 CMS8S6980-SSOP20 Pin diagram



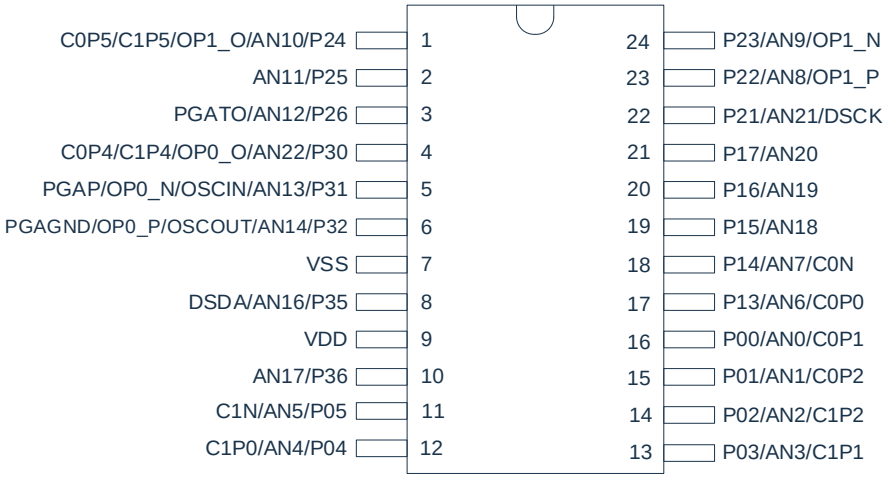
3.1.3 CMS8S6990N-TSSOP20 Pin diagram



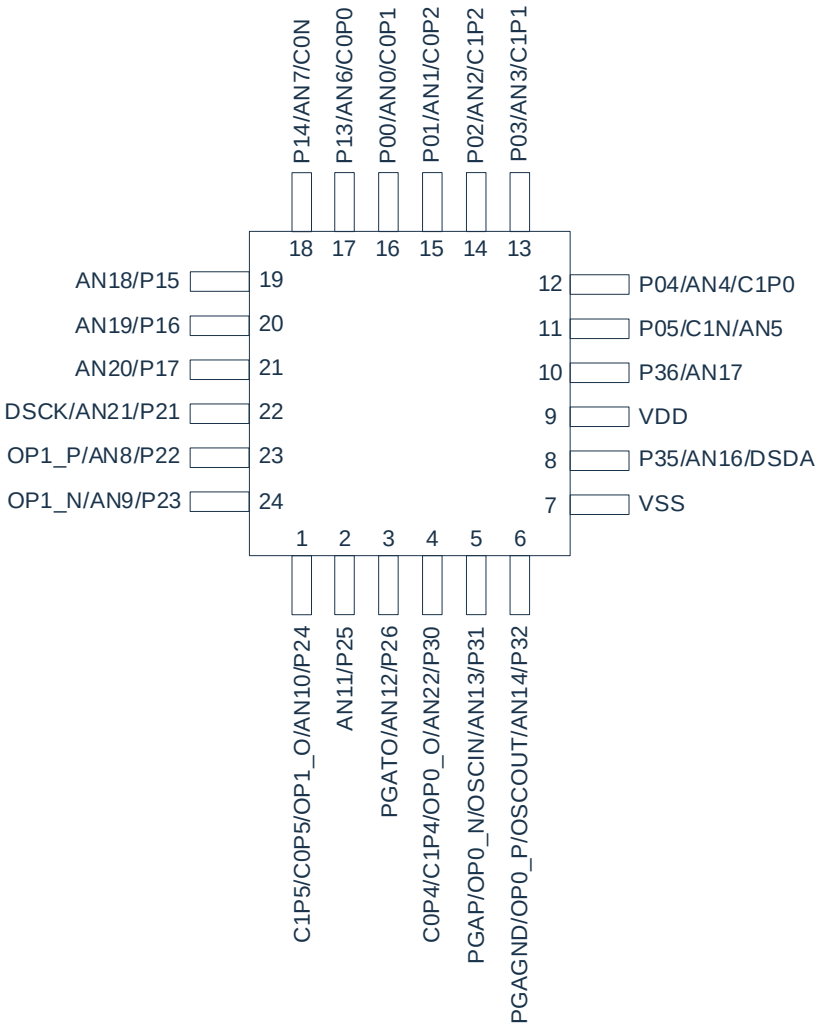
3.1.4 CMS8S6990NA-QFN20 Pin diagram



3.1.5 CMS8S6990-SSOP24 Piin diagram



3.1.6 CMS8S6990-QFN24 Pin diagram



3.2 Pin function description

Pin number						Pin Function	Pin Type	Pin description
CMS8S3680-SSOP16	CMS8S6980-SSOP20	CMS8S6990N-TSSOP20	CMS8S6990NA-QFN20	CMS8S6990-SSOP24	CMS8S6990-QFN24			
-	8	-	11	16	16	P00	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN0	I	ADC channel 0 input
						C0P1	I	Comparator 0 positive terminal channel 1 input
-	7	-	10	15	15	P01	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN1	I	ADC channel 1 input
						C0P2	I	Comparator 0 positive terminal channel 2 input
-	6	-	9	14	14	P02	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN2	I	ADC channel 2 input
						C1P2	I	Comparator 1 positive terminal channel 2 input (CMS8S6980 does not have this function)
-	5	-	8	13	13	P03	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN3	I	ADC channel 3 input
						C1P1	I	Comparator 1 positive end channel 1 input (CMS8S6980 does not have this function)
3	4	12	7	12	12	P04	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN4	I	ADC channel 4 input
						C1P0	I	Comparator 1 positive terminal channel 0 input (CMS8S3680, CMS8S6980 have no such function)
2	3	11	6	11	11	P05	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN5	I	ADC channel 5 input
						C1N	I	Comparator 1 negative terminal channel input (CMS8S3680, CMS8S6980 do not have this function)
4	9	13	12	17	17	P13	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN6	I	ADC channel 6 input
						C0P0	I	Comparator 0 positive terminal channel 0 input (CMS8S3680 does not have this function)
-	10	14	13	18	18	P14	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN7	I	ADC channel 7 input
						C0N	I	Comparator 0 negative terminal channel input
-		15	-	19	19	P15	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN18	I	ADC channel 18 input
-	-	16	-	20	20	P16	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN19	I	ADC channel 19 input
5	-	17	-	21	21	P17	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN20	I	ADC channel 20 input
6	11	18	14	22	22	P21	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN21	I	ADC channel 21 input

Pin number						Pin Function	Pin Type	Pin description
CMS8S3680-SSOP16	CMS8S6980-SSOP20	CMS8S6990N-TSSOP20	CMS8S6990NA-QFN20	CMS8S6990-SSOP24	CMS8S6990-QFN24			
						DSCK	I/O	Programming and debugging clock input and output
7	12	19	15	23	23	P22	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN8	I	ADC channel 8 input
						OP1_P	I	Op amp 1 positive input (CMS8S3680, CMS8S6980 do not have this function)
8	13	20	16	24	24	P23	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN9	I	ADC channel 9 input
						OP1_N	I	Op amp 1 negative terminal input (CMS8S3680, CMS8S6980 do not have this function)
9	14	1	17	1	1	P24	I/O	GPIO CONFIGURES INPUT AND OUTPUT PULL UP, DOWN AND OTHER FUNCTIONS THROUGH REGISTERS
						AN10	I	ADC channel 10 input
						C0P5	I	Comparator 0 positive terminal channel 5 input (CMS8S3680 does not have this function)
						C1P5	I	Comparator 1 positive terminal channel 5 input (CMS8S3680, CMS8S6980 have no such function)
						OP1_O	O	Op amp 1 output (CMS8S3680, CMS8S6980 have no such function)
10	-	2	18	2	2	P25	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN11	I	ADC channel 11 input
11	15	3	19	3	3	P26	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN12	I	ADC channel 12 input
						PGATO	O	PGA test output (CMS8S6980 does not have this function)
12	16	4	20	4	4	P30	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN22	I	ADC channel 22 input
						C0P4	I	Comparator 0 positive terminal channel 4 input (CMS8S3680 does not have this function)
						C1P4	I	Comparator 1 positive terminal channel 4 input (CMS8S3680, CMS8S6980 do not have this function)
						OP0_O	O	Op amp 0 output (CMS8S3680, CMS8S6980 have no such function)
13	17	5	1	5	5	P31	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN13	I	ADC channel 13 input
						OSCIN	I	External oscillator input
						OP0_N	I	Op amp 0 negative terminal input (CMS8S3680, CMS8S6980 do not have this function)
						PGAP	I	PGA positive input (CMS8S6980 does not have this function)
14	18	6	2	6	6	P32	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN14	I	ADC channel 14 input
						OSCOUT	O	External oscillator output
						OP0_P	I	Op amp 0 positive input (CMS8S3680, CMS8S6980 do not have this function)

Pin number						Pin Function	Pin Type	Pin description
CMS8S3680-SSOP16	CMS8S6980-SSOP20	CMS8S6990N-TSSOP20	CMS8S6990NA-QFN20	CMS8S6990-SSOP24	CMS8S6990-QFN24			
						PGAGND	I	PGA feedback input (CMS8S6980 does not have this function)
15	19	8	4	8	8	P35	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN16	I	ADC channel 16 input
						DSDA	I/O	Programming and debugging data input and output
-	-	10	-	10	10	P36	I/O	GPIO configures input and output pull up, down and other functions through registers
						AN17	I	ADC channel 17 input
16	20	9	5	9	9	VDD	P	Power supply voltage input pin
1	1	7	3	7	7	VSS	P	Ground pin

3.3 GPIO features

The pins share multiple functions, and each I/O port can be configured as any digital function or designated analog function. I/O as a general GPIO port has the following characteristics:

- Configurable 2 levels of I/O output rate.
- Configurable 2 levels of I/O drive current: Strong drive and weak drive
  - ✓ I_{OL1}：输出低电压(V_{OL})时的强驱动电流。
  - ✓ I_{OL2}：输出低电压(V_{OL})时的弱驱动电流。
  - ✓ I_{OH1}：输出高电压(V_{OH})时的强驱动电流。
  - ✓ I_{OH2}：输出高电压(V_{OL})时的弱驱动电流。
- Can read data latch status or pin status.
- Configurable rising edge, falling edge, double edge trigger interrupt.
- Configurable rising edge, falling edge, double edge interrupt to wake up the chip.
- Can be configured as normal input, pull-up input, pull-down input, push-pull output, open-drain output mode.

3.4 Pin function list

The digital functions of the CMS8S3680/69xx series chip pins can be assigned arbitrarily, that is, each I/O port can be assigned any digital function. The digital functions that can be assigned are shown in the table below:

Digital function	Direction	Function description
GPIO	I/O	General-purpose IO port, configure input and output through registers, pull-up and pull-down functions
CC0	O	Timer2 compare output channel 0
CC1	O	Timer2 compare output channel 1
CC2	O	Timer2 compare output channel 2
CC3	O	Timer2 compare output channel 3
TXD0	O	UART0 data output
RXD0	I/O	UART0 data input/synchronous mode data output
TXD1	O	UART1 data output
RXD1	I/O	UART1 data input/synchronous mode data output
SCL	I/O	I2C clock input and output
SDA	I/O	I2C data input and output
NSS	I/O	SPI slave mode chip select signal (input/output)
SCLK	I/O	SPI clock input and output
MOSI	I/O	SPI master sending and slave receiving
MISO	I/O	SPI master receiving and slave sending
PG0	O	PWM channel 0 output
PG1	O	PWM channel 1 output
PG2	O	PWM channel 2 output
PG3	O	PWM channel 3 output
PG4	O	PWM channel 4 output
PG5	O	PWM channel 35output
BEEP	O	Buzzer drive output
C0_O	O	Comparator 0 output
C1_O	O	Comparator 1 output
INT0	I	External interrupt 0 input
INT1	I	External interrupt 1 input
T0	I	Timer0 external clock input
T0G	I	Timer0 gate control input
T1	I	Timer1 external clock input
T1G	I	Timer1 gate control input
T2	I	Timer2 external event or gate control input
T2EX	I	Timer2 falling edge automatic reload input
CAP0	I	Timer2 input capture channel 0
CAP1	I	Timer2 input capture channel 1
CAP2	I	Timer2 input capture channel 2
CAP3	I	Timer2 input capture channel 3

Digital function	Direction	Function description
ADET	I	ADC external trigger input
FB	I	PWM external brake signal input

The analog function allocation of the pins is fixed, and each pin corresponds to a different analog function, and the pins are subject to the actual product. The simulation function distribution is shown in the following table:

PIN	CONFIG	1(ANALOG)				Priority of other digital functions
P00	-	AN0	C0P1	-	-	Highest
P01	-	AN1	C0P2	-	-	
P02	-	AN2	C1P2	-	-	
P03	-	AN3	C1P1	-	-	
P04	-	AN4	C1P0	-	-	
P05	-	AN5	C1N	-	-	
P13	-	AN6	C0P0	-	-	
P14	-	AN7	C0N	-	-	
P15	-	AN18	-	-	-	
P16	-	AN19	-	-	-	
P17	-	AN20	-	-	-	
P21	DSCK	AN21	-	-	-	
P22	-	AN8	-	OP1_P	-	
P23	-	AN9	-	OP1_N	-	
P24	-	AN10	C0P5/C1P5	OP1_O	-	
P25	-	AN11	-	-	-	
P26	-	AN12	-	-	PGATO	
P30	-	AN22	C0P4/C1P4	OP0_O	-	
P31	OSCIN	AN13	-	OP0_N	PGAP	
P32	OSCOUT	AN14	-	OP0_P	PGAGND	
P35	DSDA	AN16	-	-	-	
P36	-	AN17	-	-	-	lowest

4. Function summary

4.1 System clock

The system clock selects the clock source and clock frequency division through the settings of the system configuration register and the oscillator control register. The chip clock source can be selected from the following 4 types:

- Internal high-speed oscillation HSI (24MHz/48MHz).
- External high-speed crystal oscillator HSE (8MHz/16MHz).
- External low-speed crystal oscillator LSE (32.768KHz).
- Internal low-speed oscillation LSI (125KHz).

4.2 Reset

The reset operation is used to complete the initialization of the internal circuit of the chip, so that the system starts working from a certain state. The chip has the following reset methods:

- Power-on reset.
- External reset.
- Low voltage reset.
- Watchdog timeout reset.
- Software reset.
- CONFIG state protection reset.
- Power-on configuration monitoring reset.

Any of the above reset situations requires a certain response time, and the system provides a complete reset process to ensure the smooth progress of the reset action.

4.3 Power management

4.3.1 Operating mode

The chip has 3 different working modes to meet the power consumption requirements of different applications.

- Normal working mode: MCU is in normal working state and peripherals are operating normally.
- Idle mode IDLE: MCU is in idle mode, CPU stops working, and peripherals operate normally. This mode can be awakened by any interrupt.
- Sleep mode STOP: MCU is in sleep mode, CPU stops working, and peripherals stop working. This mode can be awakened by INT0/1 interrupt, external interrupt, WUT timing wakeup, LSE timing wakeup.

4.3.2 Power supply low voltage reset（LVR）

When the power supply voltage is lower than the set detection voltage, the system resets.

There are 4 options for low voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.3.3 Power supply low voltage detection（LVD）

The low voltage detection circuit compares the power supply voltage with the set voltage, and if the power supply voltage is lower than the set voltage, an interrupt request signal is generated.

There are 8 options for the settable detection voltage: 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V.

4.4 Interrupt control

The chip has multiple interrupt sources and interrupt vectors. The user-settable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer, PWM, I2C, SPI, UART0/1, P0/P1/P2/ P3, ACMP0/1, ADC, LVD, the actual number of interrupt sources varies by product.

The chip stipulates two interrupt priority levels, which can realize two-level interrupt nesting. When an interrupt has been responded, if a high-level interrupt sends a request, the latter can interrupt the former to achieve interrupt nesting.

4.5 Timer

4.5.1 WDT timer

The watchdog timer is an on-chip timer whose clock source is provided by the system clock. The WDT timeout will generate a reset. The watchdog reset is a protection setting of the system. When the system runs to an unknown state, the watchdog can be used to reset the system, thereby avoiding the system from entering an infinite loop. The WDT timer has the following characteristics:

- 8 levels of watchdog overflow time are selectable.
- Watchdog overflow interrupt can be set.
- Watchdog overflow reset can be set.

4.5.2 Timer counter 0/1（Timer0/1）

Timer 0 is similar in type and structure to Timer 1, and is two 16-bit up-counting timers. Timer0 has 4 working modes, Timer1 has 3 working modes, they provide basic timing and event counting operations.

In "timer mode", the timer register is incremented every 12 or 4 system cycles when the timer clock is enabled. In the "counter mode", the timing register will increase whenever it detects a falling edge on the corresponding input pin (T0 or T1). Timer0/1 has the following features:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- Can be used for gated counting function.
- Counter overflow interrupt.

4.5.3 Timer counter 2（Timer2）

Timer 2 is a 16-bit timer, which can be used for various digital signal generation and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc. Timer2 has the following characteristics:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- With reinstall prohibition, overflow auto reinstall, external pin falling edge auto reinstall function.
- Capture can be triggered by rising edge, falling edge, both edges or writing the low byte of the capture register.
- With a comparison function, this function can generate a periodic signal and a PWM waveform with a controllable duty cycle.
- Interrupts can be generated for timing, external trigger, capture, and comparison.

4.5.4 Timer 3/4（Timer3/4）

Timer 3/4 is similar to timer 0/1 and is two 16-bit timers. Timer3 has 4 working modes, and Timer4 has 3 working modes. Compared with Timer0/1, Timer3/4 only provides timing operation.

When the timer is started, the value of the register (counter) is incremented every 12 or 4 system cycles.

4.5.5 LSE timer

The LSE timer is a 16-bit up-counting timer with a clock source from the external low-speed clock LSE. The LSE timer has the following characteristics:

- Timing function.
- 16-bit timing value can be set.
- Can work normally in sleep mode.
- An interrupt can be generated when the count value is equal to the timer value.
- Timed interrupt can wake up idle mode/sleep mode.

4.5.6 Wake up timer (WUT)

WUT wake-up timer is a 12-bit, up-counting timer used for wake-up from sleep and a clock source from the internal low-speed clock LSI. After the system enters the sleep mode, the CPU and all peripheral circuits stop working, and the internal low-speed clock LSI provides the clock for the WUT counter. WUT has the following characteristics:

- The system can be woken up regularly in sleep mode.
- Count clock can be divided by 1, 8, 32, 256.
- 12-bit timing value can be set.

4.5.7 Baud rate timer (BRT)

BRT timer is a 16-bit baud rate timer (its clock source is from the system clock). It mainly provides the clock for the UART module. BRT has the following characteristics:

- With independent control switch.
- Counting clock has 8 frequency division options.
- 16-bit up counting.

4.6 Enhanced digital peripherals

4.6.1 BUZZER

The buzzer driver is composed of an 8-bit counter, a clock driver, and a control register. It outputs a square wave with a duty cycle of 50%, and its frequency covers a wide range. BUZZER has the following characteristics:

- With separate enable control switch.
- A total of 4 levels of system clock divider ratios of 8, 16, 32, 64 can be set.
- Output frequency 8-bit control, can be set (1~255) x 2 frequency division output.

4.6.2 Enhanced PWM module

The enhanced PWM module supports 6 PWM generators, and the period and duty cycle can be set independently. PWM has the following characteristics:

- Support 2 kinds of waveform output in single and continuous mode.
- Support 4 control modes: independent, complementary, synchronous and group control.
- Count clock can be divided by 1, 2, 4, 8, 16.
- Support two counting modes: edge alignment and center alignment, symmetrical and asymmetrical counting are supported in center alignment mode.
- Support mask output.
- Support dead zone programming.
- Output polarity can be set.
- Support cycle, compare up, compare down, zero interrupt.
- Support software brake, external port trigger brake, ADC comparison result trigger brake, ACMP output trigger brake.

4.7 Communication module

4.7.1 SPI module

SPI is a fully configurable SPI master/slave device that allows users to configure the polarity and phase of the serial clock signal. SPI allows the MCU to communicate with serial peripherals, and it can also communicate between processors in a multi-host system. SPI has the following characteristics:

- Full-duplex synchronous serial data transmission.
- Support master/slave mode.
- Support multi-host system.
- System error detection.
- Support speed up to 1/4 of the system clock (FSYS≤24MHz).
- Bit rate generates 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 of the system clock.
- Support four transmission formats.
- Send/receive complete can generate interrupt.

4.7.2 I²C module

The two-wire bidirectional serial bus controller I2C provides a simple and effective connection method for data exchange between the microprocessor and the I2C bus. The I2C module has the following characteristics:

- Support 4 working methods: master sending, master receiving, slave sending, slave receiving.
- Support 2 transmission speed modes:
  Standard (up to 100Kb/s);
  Fast （up to 400Kb/s）.
- Perform arbitration and clock synchronization.
- Support multi-host system.
- The host method supports 7-bit addressing mode and 10-bit addressing mode on the I2C bus (software support).
- The slave method supports 7-bit addressing mode on the I2C bus.
- Allows operation in a wide range of clock frequencies (built-in 8-bit timer).
- An interrupt can be generated when receiving/sending is complete.

4.7.3 UARTn module

The UARTn module contains UART0 / UART1. UARTn has the following characteristics:

- Full-duplex serial port.
- Support synchronous mode.
- Support 8-bit asynchronous transceiver mode with variable baud rate.
- Support 9-bit asynchronous transceiver mode with variable baud rate.
- Baud rate can be generated by Timer1/Timer4/Timer2/BRT module.
- Send/receive complete can generate interrupt.

4.8 Analog module

4.8.1 Analog to digital conversion（ADC）

ADC module is a 12-bit successive approximation analog-to-digital converter. The port analog input signal is connected to the input of the analog-to-digital converter after passing through the multiplexer. The analog-to-digital converter generates a 12-bit binary result according to the input analog signal and saves the result in the ADC result register. ADC has the following characteristics:

- All I/O ports can be used as external input channels of ADC.
- ADC conversion clock has 8 clock frequencies to choose from.
- ADC reference voltage can choose VDD/1.2V/2.0V/2.4V/3.0V.
- A complete 12-bit conversion requires 18.5 ADC conversion cycles.
- Support external port edge, enhanced PWM trigger ADC conversion.
- Support ADC conversion result comparison output, comparison output can control enhanced PWM brake function.
- Support ADC conversion completion to generate interrupt.

4.8.2 Analog comparator（ACMP0/1）

The comparators ACMP0 and ACMP1 have the following characteristics:

- The positive end supports multiple input ports optional.
- The negative terminal can select port input or internal reference voltage.
- The internal reference voltage divider has a total of 16 gear selections.
- Support output filtering, a total of 11 filter time options.
- Support unilateral and bilateral hysteresis control.
- Hysteresis voltage optional 10/20/60mV.
- Support offset voltage software trimming.
- The output can be used as an enhanced PWM brake trigger signal.
- Support output change to generate interrupt.

4.8.3 Operational amplifier（OP0/1）

Operational amplifiers OP0 and OP1 have the following characteristics:

- The positive end supports internal 1.2V voltage input.
- Supports comparison and op amp modes.
- The output can be connected to the internal ACMP input for shaping.
- The output can be connected to ADC channel 31 for measurement.
- Support offset voltage software trimming.

4.8.4 Programmable Operational Amplifier（PGA）

Programmable operational amplifier PGA has the following characteristics：

- Multi-stage gain is optional (1/2/4/8/16/32/64/128).
- PGA input with sample and hold circuit.
- Support single-ended/pseudo-differential input.
- Support PGA output test.
- PGA output can be connected to the internal analog comparator input for shaping.
- PGA output can be connected to ADC internal channel 31 for measurement.
- Support offset voltage software trimming.

4.9 FLASH

FLASH memory includes program memory (APROM) and non-volatile data memory (Data FLASH), which can be accessed through related special function registers (SFR) to realize IAP function. FLASH memory supports the following operations:

- Byte read operation.
- Byte write operation.
- Page erase operation.

4.10 Unique ID（UID）

Each chip has a 96-bit unique identification number, namely Unique identification. The UID has been set at the factory and cannot be modified by the user.

5. User Configuration

The system configuration register (CONFIG) is the FLASH option of the MCU's initial conditions, and the program cannot access and operate it. The following contents can be set through the system configuration register:

- Watchdog's working method.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Low voltage reset voltage.
- Disable or enable debug mode.
- Oscillation method, prescaler selection.
- Internal high-speed oscillator frequency division selection.
- External reset configuration, port selection.
- Sleep wake-up waiting time.

6. Electrical parameters

Unless otherwise specified, the temperature condition T_A of the following parameters is 25 ℃.

6.1 Absolute maximum rating

symbol	parameter	min.	max.	unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Working temperature	-40	105	℃
VDD-VSS	Power supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	120	mA
I_{IO}	Maximum sink current of a single IO	-	50	mA
	Maximum source current of a single IO	-	40	mA
	Maximum sink current of all IOs	-	120	mA
	Maximum source current of all IOs	-	120	mA

Note: If the operating conditions of the device exceed the range of "**absolute maximum rating**", it will cause permanent damage to the device. The function can be guaranteed only when the device works within the scope specified in the manual. The chip is at the absolute maximum rated value, which may affect the reliability of the device.

6.2 DC electrical characteristics

VDD-VSS=2.1～5.5V, T_A=25℃

symbol	parameter	test condition	min.	typical	max.	unit
VDD	Working voltage	F_{SYS}=48MHz, machine cycle=2T F_{SYS}=8MHz~24MHz, machine cycle=1T	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals are off machine cycle=2T	-	6	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals are off machine cycle=2T	-	6	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off machine cycle=1T	-	4	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off machine cycle=1T	-	4	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off machine cycle=1T	-	3	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off machine cycle=1T	-	3	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals are off machine cycle=1T	-	2	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off machine cycle=1T	-	2	-	mA
	IDLE mode	VDD=5V, F_{SYS}=48MHz, all peripherals are off	-	4	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals are off	-	4	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off	-	2.5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off	-	2.5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off	-	2	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off	-	2	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals are off	-	1.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off	-	1.5	-	mA
I_{SLEEP1}	sleep current	VDD=3V , all peripherals are off, LSE、LSE timer enable	-	20	-	uA
I_{SLEEP2}	sleep current	VDD=3V , all peripherals are off, LSI、WUT timer enable	-	7	-	uA
I_{SLEEP3}	sleep current	VDD=3V, all peripherals are off	-	6	-	uA
I_{LI}	Input leakage	-	-1	-	1	uA
V_{IL}	Input low level	-	VSS	-	0.3VDD	V
V_{IH}	Input high level	-	0.7VDD	-	VDD	V
V_{OL}	Low output voltage	VDD=5V, I_{OL1}=12mA	-	-	0.4	V
		VDD=5V, I_{OL2}=7mA	-	-	0.4	V
		VDD=3V, I_{OL1}=9mA	-	-	0.4	V
		VDD=3V, I_{OL2}=5mA	-	-	0.4	V
V_{OH}	Output high voltage	VDD=5V, I_{OH1}=40mA	3.5	-	-	V
		VDD=5V, I_{OH2}=20mA	3.5	-	-	V
		VDD=3V, I_{OH1}=15mA	2.1	-	-	V
		VDD=3V, I_{OH2}=8mA	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

6.3 AC electrical parameter

6.3.1 Power-up and power-down operations

TA=25℃, does not include 32.768K crystal oscillator start-up time

symbol	parameter	test condition	min.	typical	max.	unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	us/V

6.3.2 External oscillator

symbol	parameter	test condition	min.	typical	max.	unit
V_{HSE}	Working voltage	F=8/16MHz,C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Working voltage	F=32.768KHz,C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal oscillator

VDD=2.1V-5.5V

symbol	parameter	test condition	Frequency error	min.	typical	max.	unit
F_{HSI}	Internal high speed 48MHz	T_A=25℃	±1%	-	48	-	MHz
		T_A=-20℃ to 85℃	±2%	-	48	-	MHz
		T_A=-40℃ to 105℃	±3%	-	48	-	MHz
F_{LSI}	Internal high speed 125KHz	T_A=25℃	±20%	-	125	-	KHz
		T_A=-40℃ to 105℃	±50%	-	125	-	KHz

6.3.4 Low voltage reset electrical parameter

symbol	parameter	min.	typical	max.	unit
V_{LVR1}	Low pressure detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low pressure detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low pressure detection threshold 3.5V	3.35	3.5	3.65	V

6.3.5 LVD electrical parameter

symbol	parameter	min.	typical	max.	unit
V_{LVD1}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low pressure detection threshold 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low pressure detection threshold 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low pressure detection threshold 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low pressure detection threshold 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low pressure detection threshold 3.7V	3.55	3.7	3.85	V
V_{LVD7}	Low pressure detection threshold 4.0V	3.85	4.0	4.15	V
V_{LVD8}	Low pressure detection threshold 4.3V	4.15	4.3	4.45	V

6.4 FLASH electrical parameter

symbol	parameter	test condition	min.	typical	max.	unit
V_F	FLASH working voltage	-	2.1	-	5.5	V
T_F	FLASH working temperature	-	-40	25	105	℃
$N_{ENDURANCE}$	Number of erasing and writing	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	1.5	-	ms
T_{WRITE}	Write time	-	-	30		us
T_{READ}	Read time	-	-	3*Tsys	-	-
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erase current	-	-	-	2	mA

6.5 Analog characteristics

6.5.1 BANDGAP electrical characteristics

T_A=25℃

symbol	parameter	test condition	min.	typical	max.	unit
V_{BG}	Internal reference 1.2V	VDD=2.1~5.5V、T_A=25℃	1.188	1.2	1.212	V
		VDD=2.1~5.5V、T_A=-20℃ to 85℃	1.182	1.2	1.218	V
		VDD=2.1~5.5V、T_A=-40℃ to 105℃	1.176	1.2	1.224	V

Note: The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured for mass production.

6.5.2 ADC electrical characteristics

T_A=25℃

symbol	parameter		min.	typical	max.	unit
V_{AVDD}	ADC working voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2(Note1, Note2)（Not V_{BG}）		1.185	1.2	1.215	V
V_{REF3}	Reference voltage 3(Note2)		1.985	2.0	2.015	V
V_{REF4}	Reference voltage 4(Note2)		2.385	2.4	2.415	V
V_{REF5}	Reference voltage 5(Note2)		2.985	3.0	3.015	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	resolution		12			Bit
DNL	Differential nonlinearity error（V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us）		±2			LSB
INL	Integral nonlinearity error（V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us）		±4			LSB
T_{ADCK}	ADC clock cycle	V_{REF}=VDD=5V	0.5	-	-	us
		V_{REF}=V_{REF2}	32	-	-	us
		V_{REF} =V_{REF3}/ V_{REF4}/V_{REF5}	2	-	-	us
T_{ADC}	ADC conversion time		-	18.5	-	T_{ADCK}
F_S	Sampling rate（V_{REF}=V_{AVDD}=5V）		100			Ksps

Note1: When V_{REF}=V_{REF2}, the precision is 8bit.
Note2: Test Condition: T_A=25°C, V_{AVDD}=5.0V.

6.5.3 ACMP Eelectrical characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless otherwise stated

symbol	parameter	condition	min.	typical	max.	unit
VDD	Power supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.2	0.3	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Working temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Not zeroed (CnADJ=10H)	-	±4.0	-	mV
		Zeroed	-	±0.5	±1.0	
V_{CM}	Common mode input voltage range	-40℃~105℃	-0.1	-	VDD-1.5	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	85	-	dB
BW	Bandwidth	-	-	150	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V -40℃~105℃	-	90	-	dB
Transient characteristics						
T_{STB}	Stabilization time	-	-	-	5	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

Note: Design assurance.

6.5.4 OP electrical characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, VIN+=1V, unless otherwise stated

symbol	parameter	condition	min.	typical	max.	unit
VDD	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0mV	-	1.0	1.6	mA
I_{SD}	Shutdown current	-	-	5	-	nA
T_A	Working temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Not zeroed (OPnADJ=10H)	-	±3.5	-	mV
		Zeroed	-	±0.5	±1.0	
V_{CM}	Common mode input voltage range	-40℃~105℃	0	-	VDD-1.5	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
Output characteristics						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃, I_{LOAD}=0.1mA	-	-	VDD-0.1	
		-40℃~105℃, I_{LOAD}=1mA	-	-	VDD-0.3	V
V_{OL}	Minimum output voltage	-40℃~105℃, I_{LOAD}=0.1mA	0.1	-	-	
		-40℃~105℃, I_{LOAD}=1mA	0.3	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	80	-	dB
BW	Bandwidth	R_{LOAD}=2K,C_{LOAD}=100pF	-	5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	75	-	dB
CMRR	Common mode rejection ratio	V_{IN+}=0.3~（VDD-1.5） -40℃~105℃	-	90	-	dB
Transient characteristics						
SR	Slew rate	R_{LOAD} =2K,C_{LOAD} =100pF	-	±8	-	V/μs
T_{STB}	Stabilization time	-	-	-	2	μs

Note: Design assurance.

6.5.5 PGA electrical characteristics

T_A＝25℃, VDD＝5V, V_{IN+}=0.01V, unless otherwise stated.（G is the gain multiple）

symbol	parameter	condition	min.	typical	max.	unit
VDD	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{OUT}=2V	-	0.5	0.7	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Working temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	Not zeroed (PGAADJ=20H)	-	±2.5	-	mV
		Zeroed	-	±0.1	±0.2	
V_{CM}	Common mode input voltage range	G=1	0.064	-	(VDD-1.8)/ G	V
		G=2	0.032			
		G=4	0.016			
		G=8	0.008			
		G=16	0.005			
		G=32, 64,128	0.005			
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Gain error	G=1, 2, 4, 8, 16	-1	-	1	%
		G=32	-2	-	2	
		G=64,128	-4	-	4	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃ (Internal output)	-	-	VDD-1.8	V
V_{OL}	Minimum output voltage	-40℃~105℃ (Internal output)	0.064	-	-	V
Frequency characteristics						
BW	Bandwidth	C_{LOAD}=10pF,G=1	-	1.5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V,G=16	-	75	-	dB
CMRR	Common mode rejection ratio	-40℃~105℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	C_{LOAD}=10pF,G=32 (Internal output)	-	10	-	V/μs
T_{STB}	Stabilization time	Internal output	-	-	2	μs
$T_{SH(1)}$	Sample hold time	Internal output	-	3	-	μs

Note: Design assurance.

6.6 EMC Characteristics

6.6.1 EFT electrical characteristics

symbol	parameter	test condition	level
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDDand VSSpins to induce a functional disturbance	T_A = + 25°C, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4B

Note: The electrical fast transient (EFT) immunity performance is closely related to system design (including power supply structure, circuit design, layout, chip configuration, program structure, etc.). The EFTparameter in the above table is the result measured on the CMS internal test platform, and is not suitable for all application environments. The test data is only for reference. All aspects of system design may affect EFT performance. In applications with high EFT performance requirements, attention should be paid to avoid interference sources affecting system operation when designing. It is recommended to analyze interference paths and optimize the design to achieve the best anti-interference performance.

6.6.2 ESD Electrical characteristics

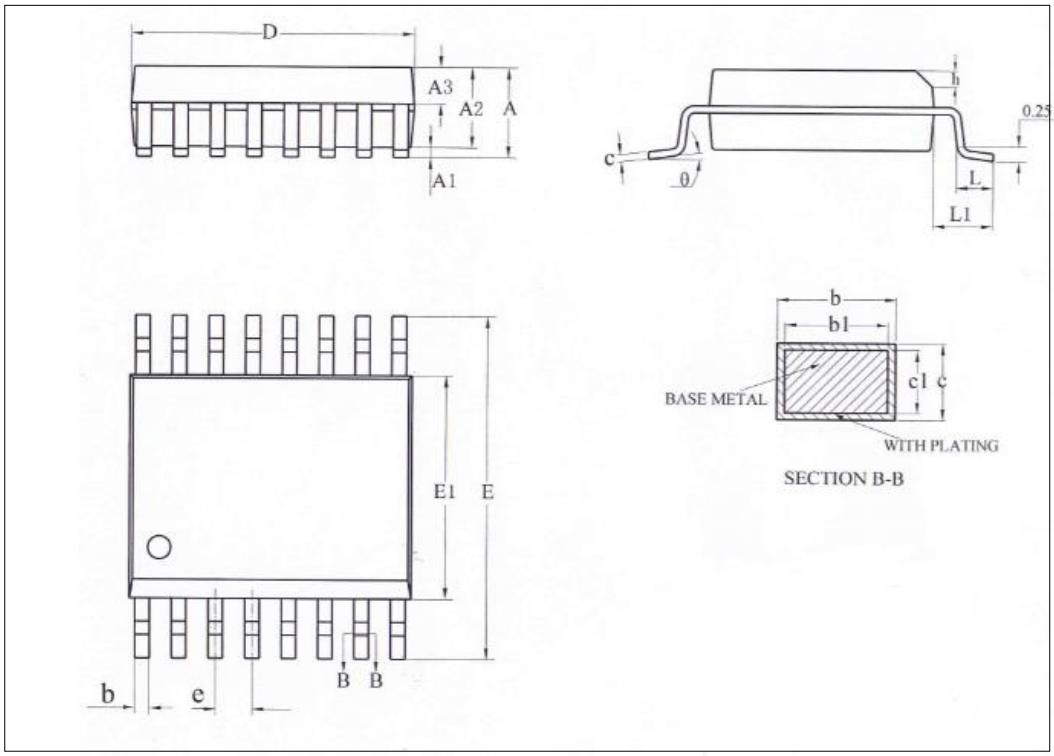
symbol	parameter	test condition	level
V_{ESD}	Electrostatic discharge (Human body model HBM)	T_A = + 25°C, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (Machine discharge mode MM)	T_A = + 25°C, JEDEC EIA/JESD22- A115	C

6.6.3 Latch-Up electrical characteristics

symbol	parameter	test condition	Test type
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25°C)

7. Package information

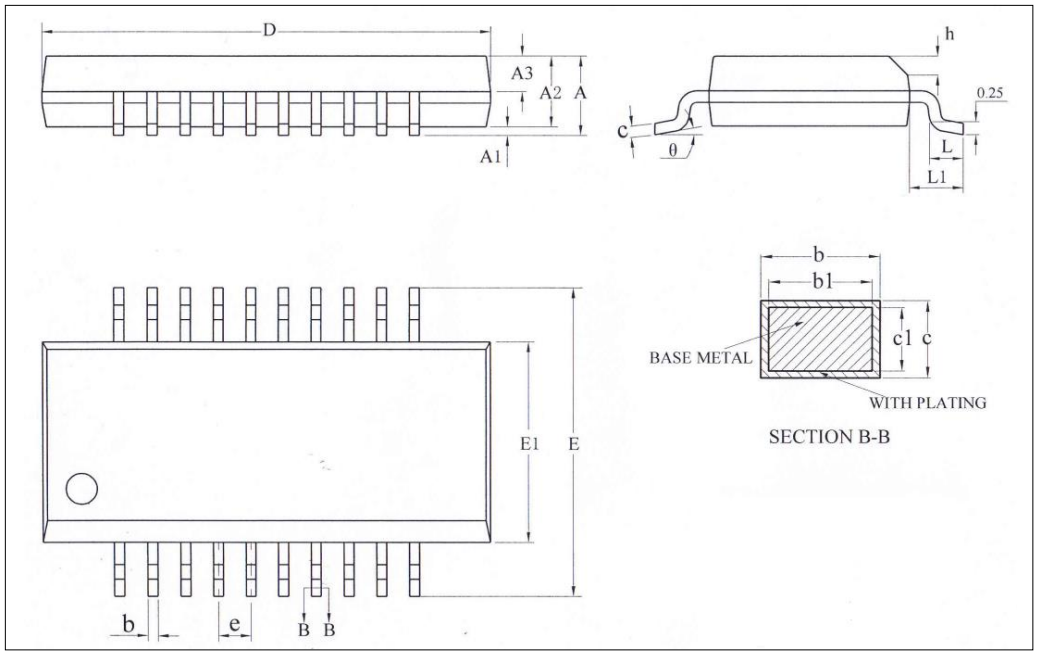
7.1 SSOP16 (0.635mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	-	0.50
L	0.50	0.65	0.80
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

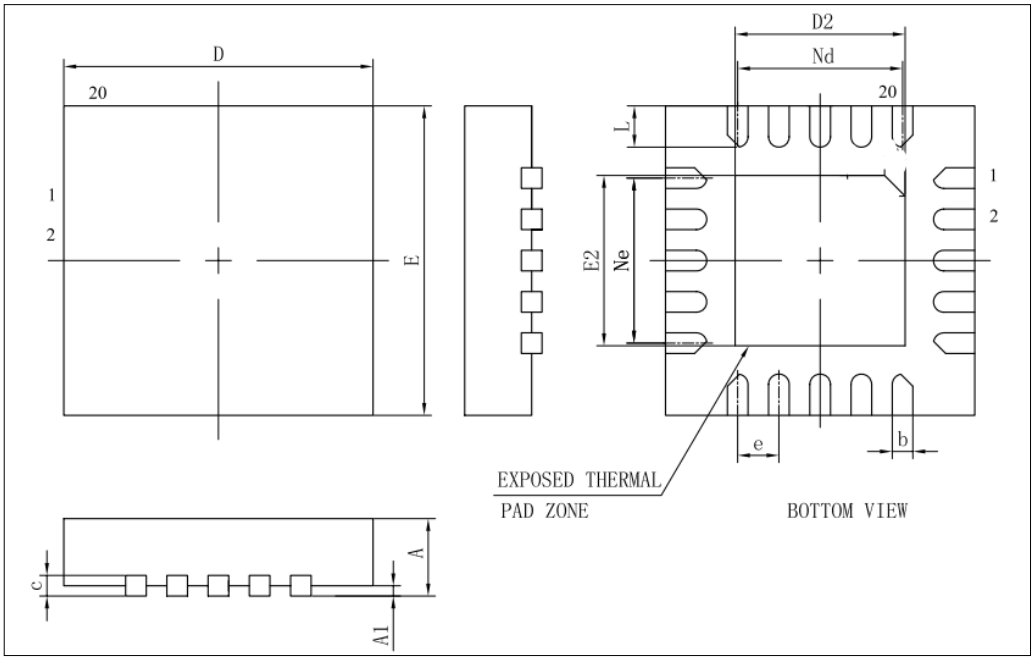
7.2 SSOP20



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

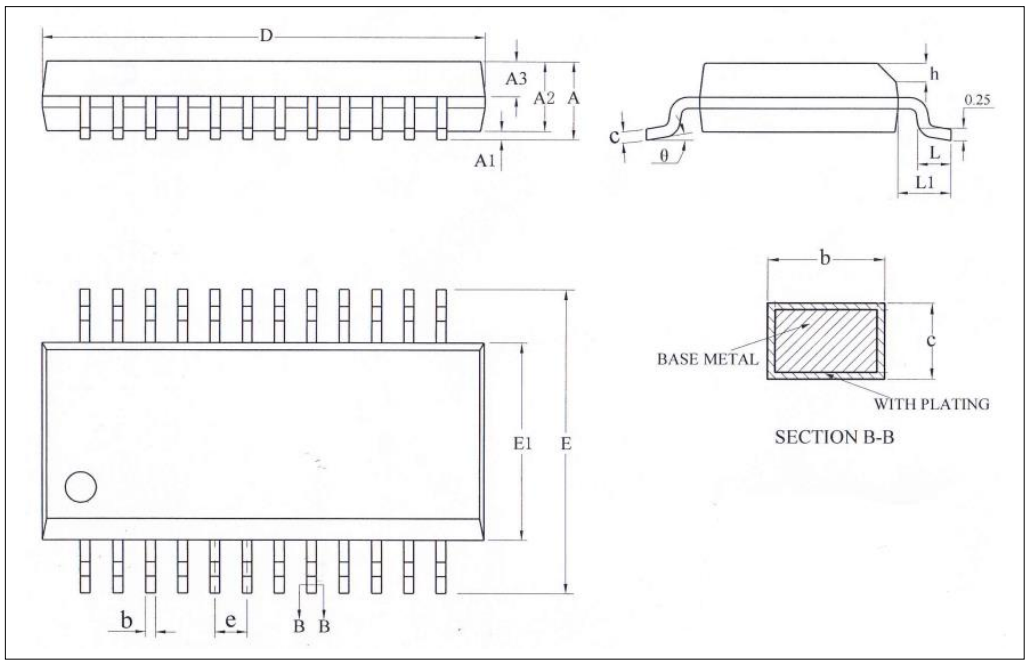
7.3 QFN20 (3x3x0.75-0.40mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.65	0.75	0.85
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	-	2.00
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	-	2.00
L	0.20	-	0.50

Caution: Package dimensions do not include mold flash or gate burrs.

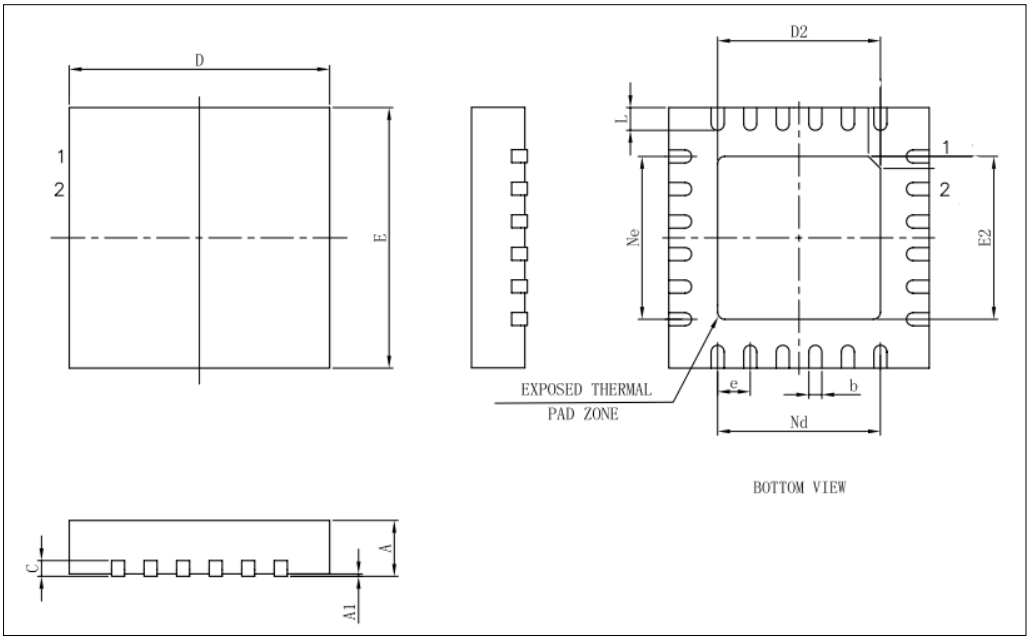
7.4 SSOP24



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.80
A1	0.10	0.15	0.25
A2	1.30	-	1.55
A3	0.60	0.65	0.70
b	0.20	-	0.31
c	0.20	-	0.24
D	8.53	-	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.406	-	0.889
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

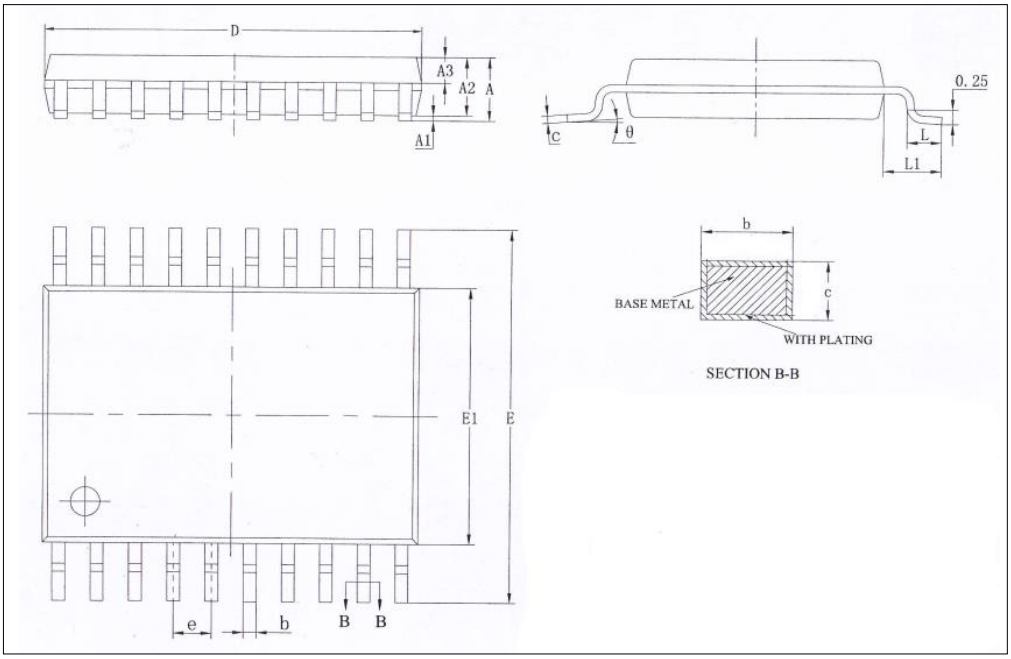
7.5 QFN24 (4x4x0.75-0.50mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.20	-	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.20	-	2.80
L	0.30	0.40	0.50
h	0.25	-	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

7.6 TSSOP20



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.25
A1	0.05	-	0.15
A2	0.80	1.00	1.10
A3	0.34	0.44	0.54
b	0.20	-	0.28
c	0.10	-	0.19
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

8. Version history

Version	Time	Revised cotent
V1.00	Jan 2020	Initial verison
V1.01	Aug 2020	Update electrical parameters and some model descriptions
V1.02	Nov 2020	Content update and part model description
V1.05	Feb 2023	1) 6.4 Correct FLASH electrical parameters 2) 6.1 Absolute maximum rating: add limit parameter notes 3) Modify 6.2 DC electrical characteristics 4) 6.3.1 Power-on and power-off operation: adjust parameters 5) 6.3.3 Internal oscillator: adjust parameters 6) 6.3.4 FLASH electrical parameters: optimize the description of writing and reading time 7) 6.5.1 BANDGAP electrical characteristics: detailed parameters 8) 6.5.2 ADC electrical characteristics: ADC clock cycle is described according to different reference voltages 9) 6.5.3 ACMP electrical characteristics: optimize parameters, add notes 10) 6.5.4 OP electrical characteristics: optimize parameters and add notes 11) 6.5.5 PGA electrical characteristics: optimize parameters and add notes 12) 6.1 Absolute maximum rated value: maximum pulling current of single IO 13) 6.5.1 BANDGAP electrical characteristics: add notes 14) 3.3 GPIO characteristics: add description of driving current I_{OL1}, I_{OL2}, I_{OH1} and I_{OH2} 15) Optimization description
V1.0.6	Apr 2023	1) Update 7.1 Packaging Dimensions 2) Correct 7.2 Packaging Dimensions 3) Update 6.6EMC Characteristics
V1.0.7	Sep 2024	1) Adjusted the format of the pinout diagram 2) Correct 2.2.3 Memory address 3) Revised the cover page
	Oct 2024	Modified SSOP20/QFN20/SSOP24/QFN24/TSSOP20 package dimensions
V1.0.8	Dec 2024	Added Remarks in section 6.5.2